January 25, 2018

NEWS RELEASE

Development of HRDP™ Material for Formation of Ultra-Fine Circuits with Glass Carrier for Fan Out Panel Level Package

- Aiming for mass production in collaboration with GEOMATEC Co., Ltd. -

Mitsui Mining & Smelting Co., Ltd. (President: Keiji Nishida; "Mitsui Kinzoku," hereinafter) is pleased to announce that it has developed HRDP™*1 material for the formation of ultra-fine circuits with glass carrier for Fan Out Panel Level Packaging and established its mass production technology with GEOMATEC Co., Ltd. (President: Kentaro Matsuzaki; "GEOMATEC" hereinafter).

Mitsui Kinzoku's MicroThin™*2 ultra-thin copper foil is widely used in packaged circuits for smartphones and other devices to meet the high performance requirements of the IoT age as a material for the formation of ultra-fine circuits using the MSAP*3 method. In addition, the SAP method*4, using ultra-thin copper foil for the formulation of ultra-fine circuits, has today been commercially implemented. As a technology that surpasses the limits of these methods, Fan Out Wafer Level Packaging (FO-WLP*5) based on the Chip-First Process*6 is attracting attention, however, it is concerned that yield instability caused by a loss of known good dies on this process nature would end up with a significant increase in total costs.

Currently, focus of attention is becoming more on Fan Out Panel Level Package *7 based on the RDL-First process*8 to place known good dies on the good redistribution layer (RDL) with a panel level format that could potentially lower the cost of fan-out technology. To accelerate the momentum to bring the lower cost fan-out technology in to market, Mitsui Kinzoku has recently developed HRDP™ as a material that make Fan Out Panel Level Package happen.

It is confirmed that ultra-fine circuits with a line/space (L/S) ratio of around 2/2 μm*9 may be produced using this product. Evaluations for HRDP are now in progress at a number of electronic device manufacturers and supply chains for the IC packaging houses.

Under its slogan of Material Intelligence, Mitsui Kinzoku will create products in collaboration with GEOMATEC, which owns excellent thin-film formation technologies, in a bid to realize customers' wishes to ensure stable quality and sufficient supply.

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(Notes)

*1 High Resolution De-bondable Panel
(For details, refer to Appendix: *Introduction to Technologies*.)

*2 MicroThin™ is Mitsui Kinzoku's ultra-thin copper foil with carrier.

*3 Modified Semi-Additive Process

*4 Semi-Additive Process

*5 Fan Out Wafer Level Package

*6 The method in which the process of placing semiconductor chips onto the carrier is performed first.

*7 Fan Out Panel Level Package (For details, refer to Appendix: *Introduction to Technologies*.)

*8 The method in which the process of forming the redistribution layer (RDL) is performed first.
(For details, refer to Appendix: *Introduction to Technologies*.)

*9 The line width of 2 μm and the space between neighboring circuit lines of 2 μm.

Reference (as of 30 September 2017)
GEOMATEC Co., Ltd.
Location: Yokohama Landmark Tower 9F, 2-2-1 Minato Mirai, Nishi-ku, Yokohama, Japan
President: Kentaro Matsuzaki
Capital: 4,043.85 million yen
Number of Employees: 595 (consolidated), 443 (non-consolidated)
Business Activities: Manufacturing, distribution, and others of substrates for flat-panel displays (substrates for liquid crystal displays, OLED, and touchscreen panels), components for optical devices, optical components for solid-state lasers and other vacuum coating products

(Appendix)

[Introduction to Technologies]

1. HRDP™ (newly developed product)

HRDP™ has a structure in which a multilayer thin film is formed on the surface of the glass carrier (See Photo 1 and Figure 1). It is characterized in that the ultra-thin seed layer for plating formed on the very flat glass carrier enables the formation of an ultrafine redistribution layer (RDL) in panel size, for example, 600 mm by 600 mm. The release layer makes it possible to remove the mechanical glass carrier, which is stable after a thermal load at 260°C.

Photo 1: Exterior Surface of HRDP™

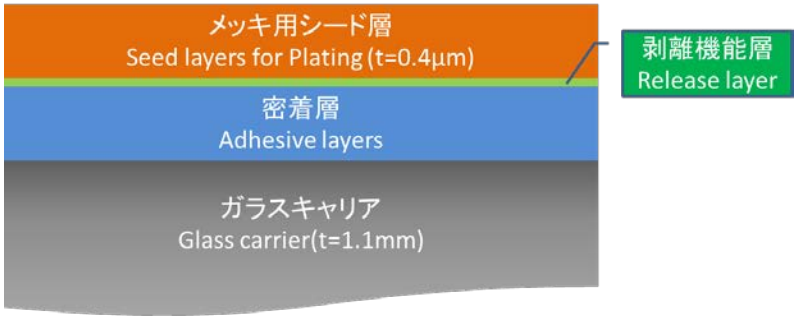


Figure 1: Schematic diagram of a cross-section of HRDP™

2. The Fan Out Panel Level Package Manufacturing Process Using HRDP™

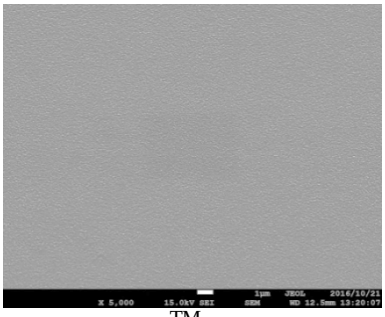
An example of the RDL-First Process using HRDP™ (See Figure 2) and Fan Out Panel Level Package structure (See Figure 3 and Photo 3) are shown below. On HRDP™, the process of photoresist formation, exposure and development, copper plating, removal of the photoresist, etching of the seed layer for plating, formation of the dielectric layer, formation via holes, and formation of the seed layer is repeated to produce the RDL. Then, a silicon chip is mounted using the flip chip technology and sealed with a mold material. The glass carrier is released between the release layer and the adhesive layer. The release layer that remains on the circuit is removed by etching. It has been confirmed that the process of circuit formation using HRDP™ achieves a line/space ratio of 2/2 μm (See Photo 3).

~ An example of RDL1st process using HRDP™ ~

1. HRDP™

↓ Seed layer, release layer, bonding layer

Glass carrier

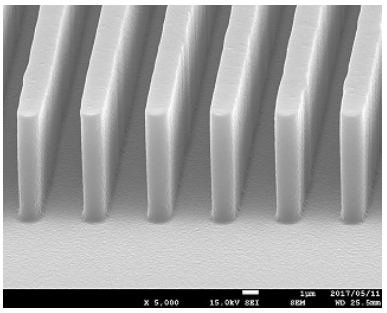


HRDP™ surface

2. Photoresist

3. Exposure and Development

↓ Photoresist

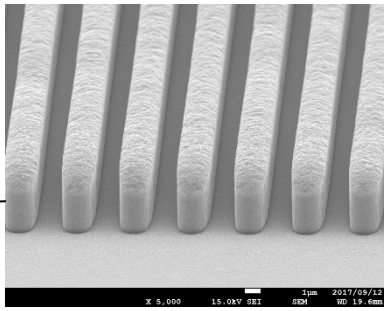


Photoresist pattern

4. Cu plating

Cu plating ↓

5. Stripping



Cu plating pattern

6. Flash etching

7. Dielectric layer

↓ Dielectric material

8. Via hole

9. Seed layer

Repeat 2~9process for 2L and 3L

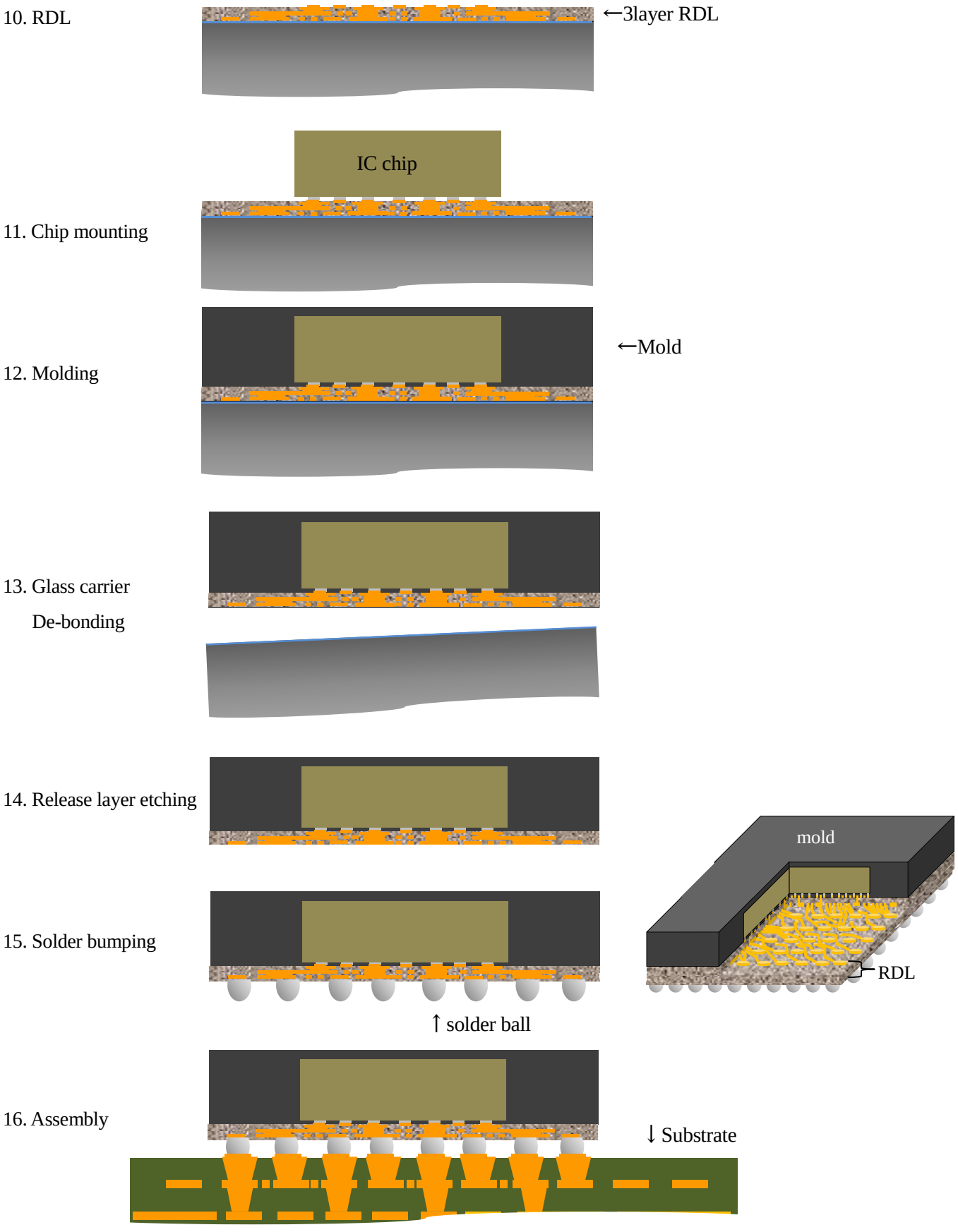
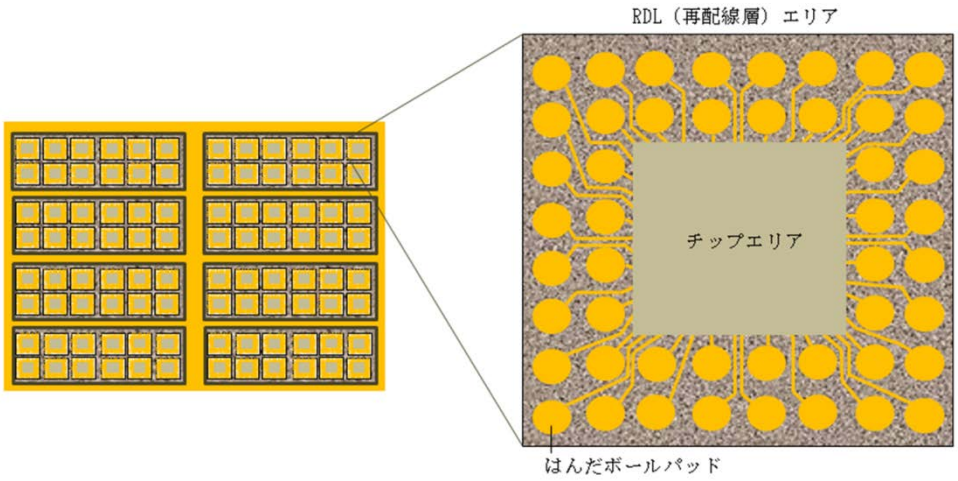


Figure 2: Example of RDL-First process using HRDP™



RDL（再配線層）エリア： Redistribution Layer (RDL) Area

チップエリア　： Chip Area

はんだボールパッド： Solder Ball Pad

Figure 3: Schematic diagrams of Fan Out Panel Level Package structure

(Left: RDL in panel size, Right: Magnified view of package)

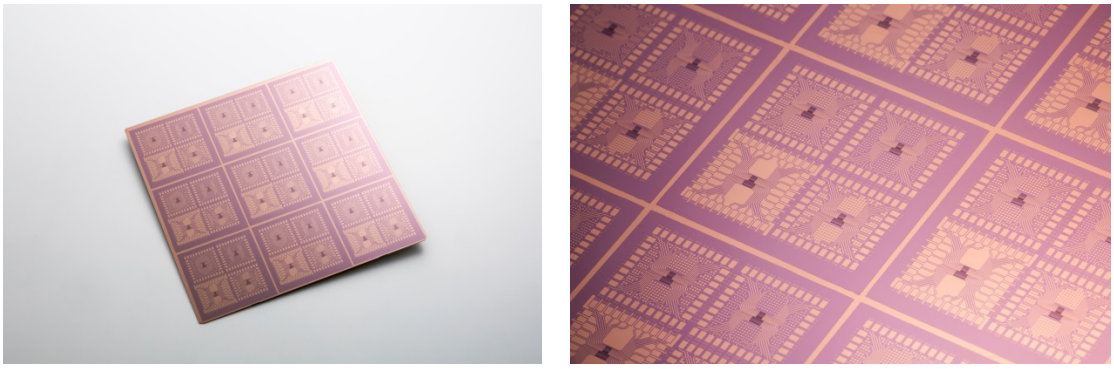


Photo 2: Exterior surface of HRDP^{TM} after circuit formation

(Left: Complete view of HRDP^{TM}, Right: Magnified view)

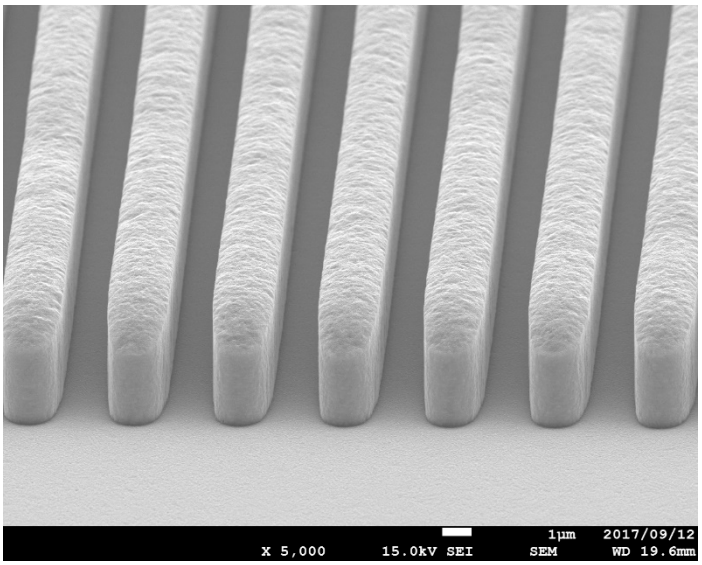


Photo 3: SEM image of circuit with L/S ratio of 2/2 µm